**Amendments to the Specification:**

Please amend the last paragraph on page 3 of the present application as follows:

Accordingly, there is a need for a system and method for transferring large amounts of complex data across a bit level network. Further, there is a need to [retaining] retain the simplicity, cost effectiveness, and reliability of the prior art bit level network while accomplishing the transfer of large amounts of complex data.

Please amend the second paragraph on page 4 of the present application as follows:

Multiple bit addresses within a time multiplexed data stream are assigned functions such as register number, data, and error detection. This establishes a data transfer frame that is used to multiplex data between a host and a module. The module includes a section of random access memory used as a register map. Communication to and from the host is accomplished through the register map. This map contains module setup information, software configuration settings, raw data, and summary data. Commands are sent from the host to the module and the module responds accordingly. The host commands the module to read registers from its map and respond with the stored register values or to write registers with the values sent. Registers are designated in the module as read only, write only, or read/write. This facilitates data protection methods.

Please amend the second full paragraph on page 8 of the present application as follows:

The frame address **35** and the channel pair or channel set **33** for the module **30** must be configured. In the illustrated embodiment, the user I/O interface **42** includes two input devices and three output devices. The input devices include a frame address [**35**] selector **44** and a channel pair or channel set [**33**] selector **46**. While the illustrated embodiment of the input devices **44, 46** common to serial multiplexed data systems is described below, those skilled in the art will recognize other embodiments which may be used without interfering with the advantages of the present invention. The output devices include a warning indicator **50**, an alarm indicator **52**, and a power indicator **54**. In one embodiment, the output indicators **50, 52, 54** are color coded light emitting diodes which

can be sequenced to flash indicating a specific message. Those skilled in the art will recognize that other output indicators could be used without interfering with the advantages of the present invention.

Please amend the second full paragraph on page 8 of the present application as follows:

Figure 3a illustrates a bitwise representation of one embodiment of a multi-bit message **60**. The message **60** includes a 16-bit Command for Module message segment **62** and a 16-bit Data for Module message segment **64**, each starting at the same frame addresses **35** on sequential or preselected multiplexed channel sets **33**. The Command for Module (CFM) message segment **62** appears on the first multiplexed channel **31** of the preselected multiplexed channel set **33.** The Data For Module (DFM) message segment **64** appears on the sequential or next multiplexed channel **37** of the preselected multiplexed channel set **33**. The format for both the CFM **62** and the DFM **64** is defined for each register **57** being addressed (bit, signed, unsigned, etc.). The bus data is from the least significant bit (LSB) to the most significant bit (MSB) with the LSB being the lowest serial multiplexed data system address. Each message segment **62, 64** is duplicated with CDR data check segments,**74** and **76** respectively, thereby making up the full 64-bit message **60**.

Please amend the first full paragraph on page 11 of the present application as follows:

Figure 4 is a flow diagram of the communications between the host **28** and the module **30**. The host begins generating a message for the module in step **100**. When communicating from the host **28** to the module **30**, the host **28** expects a response to the command during the next complete scan of the module **30** following the scan transmitting the message **60**. If the host **28** cannot ensure that it can change all 32-bits of the message **60** it is sending in one scan, as shown in step **102**, the host **28** sends a changing data indicator, step **104**, in the CFM [field] **62** while altering the DFM [field **104**] **64**. In one embodiment, the changing data indicator is the command 0xFFFF. The module **30** echoes the message **60**, step **106**, if it receives a changing data indicator in the CFM [field

**106]** 62. The host **28** supports CDR on this command as well. A complete message **60** is transmitted from the host **28** to the module **30** in step **108**.

Please amend the second full paragraph on page 11 of the present application as follows:

The module **30** receives the message **60** from the host **28** in step **110**. The message is decoded and the CDR verified in step **112**. The decoded message **60** is checked to ensure that it is not corrupt and does not contain errors in step **114**. If the message **60** is corrupt or contains errors, then appropriate remedial actions are taken in step **116**. The CFM **62** is parsed to determine whether the message **60** is a read or write request from the host **28**. For a read command, the module **30** reads the contents of the specified register in step **120** and responds with a message **60** containing the contents of the requested register on the next scan of the module **30** in step **122**. The module **30** responds to a write command from the host **28** by passing the entire received message **60** [received] back to the host **28** in step **124** and the specified register is updated with the contents of the DFM **64** in step **126**.

Please amend the first full paragraph on page 14 of the present application as follows:

Accordingly, a method and apparatus for data table multiplexing on a serial multiplex data system has been shown and described. The method used to transfer this data is a software data multiplexing protocol which uses the identical address space on two sequential data channels to send a message containing a command for a specific register on the first channel and the associated data on the second channel. The method and apparatus utilizes the previous physical layer protocol and is capable of coexisting with previous systems. Multiple bit addresses within a time multiplexed data stream are assigned functions such as register number, data, and error detection. This establishes a data transfer frame that is used to multiplex data between a host and a module.